

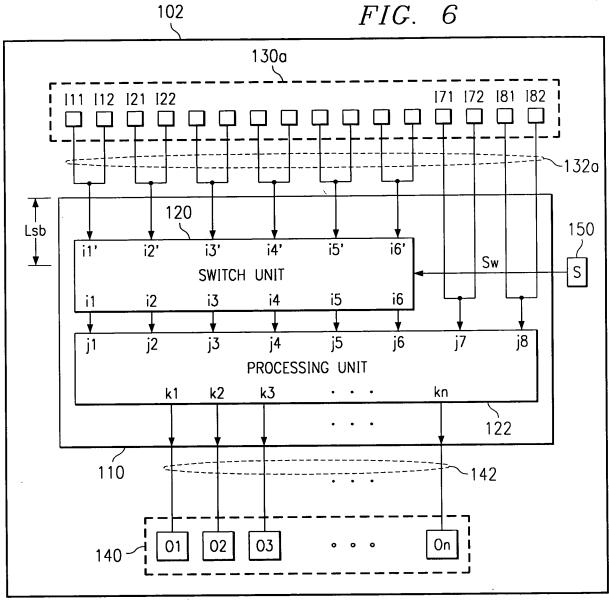
FIG. 3

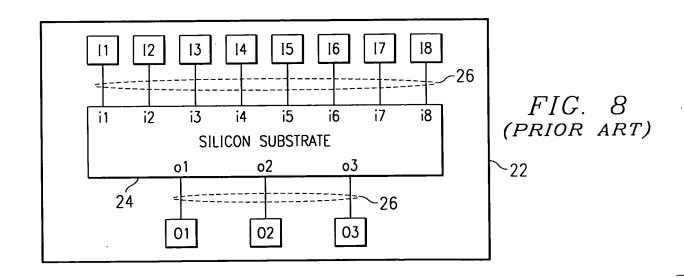
Sw	INPUT	i1'	i2'	i3'	i4'	i5'	i6'
L	OUTPUT	i1	i2	i3	i4	i5	i6
Н		i6	i5	i4	i3	i2	i1

FIG. 9 (PRIOR ART)

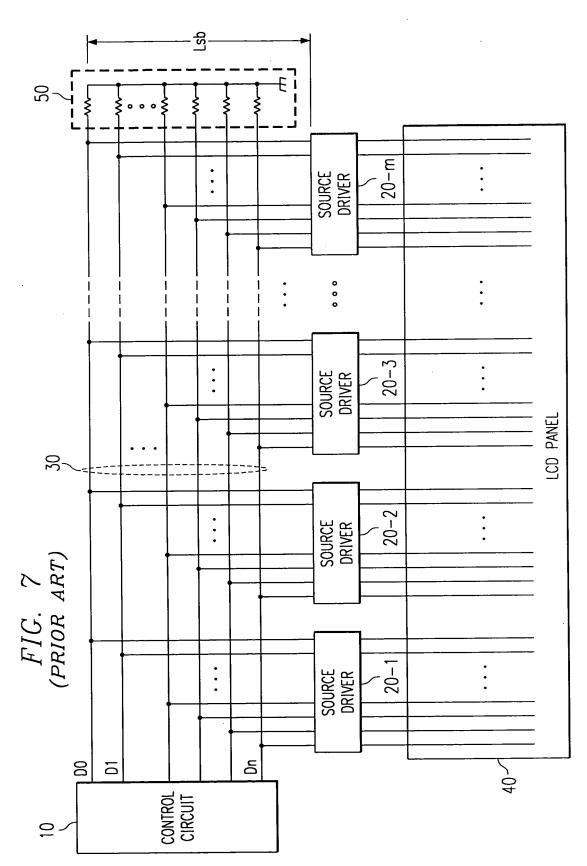
D6 — I6 D5 — I5 D4 — I4 SOURCE D3 — I3 DEVICE D2 — I2 D1 — I1	16
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3.5